

CLAIMS

I claim:

1. A system comprising:

 a plurality of components,

 a bus structure that is configured to facilitate communications among the plurality of components, and

 an activity detector that is configured to detect an initiation of a data-transfer operation and to provide therefrom an enabling signal that is communicated to a bus interface of at least one of the plurality of components,

 wherein

 the bus interface is configured to be enabled to receive data from the bus structure upon receipt of the enabling signal from the activity detector.

2. The system of claim 1, wherein

 the activity detector is further configured to detect a completion of the data-transfer operation, and terminates the enabling signal based on the completion of the data-transfer operation, and

 the bus interface is configured to be disabled from receiving data from the bus structure upon termination of the enabling signal.

3. The system of claim 1, wherein

 the enabling signal includes a gated clock signal.

4. The system of claim 1, wherein

 the bus interface includes a plurality of clocked devices that are clocked based on the enabling signal.

5. The system of claim 1, wherein

the activity detector includes:

a set-reset device that is set upon detection of the initiation of the data-transfer operation, and

a delay device, operably coupled to the set-reset device, that is configured to provide the enabling signal synchronous with a system clock that is common to the bus structure, based on whether the set-reset device is set.

6. The system of claim 5, wherein

the set-reset device is reset upon detection of a completion of the data-transfer operation.

7. The system of claim 1, further including

a bus controller that is configured to establish a communications path between an initiating component of the plurality of components and a target component of the plurality of components,

wherein

the activity detector provides the enabling signal within a time duration consumed by the bus controller to establish the communications path.

8. The system of claim 7, wherein

the bus controller includes one or more devices that operate in dependence upon the enabling signal.

9. The system of claim 1, wherein

a component of the plurality of components is configured to signal the initiation of the data-transfer operation to the activity detector before the component initiates the data-transfer operation via the bus structure.

10. A method of reducing power consumption in a system comprising a plurality of components that are configured to communicate via a bus structure, comprising:

detecting an initiation of bus activity by a component of the plurality of components, communicating an enabling signal to one or more other components of the plurality of components, and

enabling a bus interface at each of the one or more other components to receive signals corresponding to the bus activity, based on the enabling signal.

11. The method of claim 10, further including

detecting a completion of the bus activity, and

disabling the bus interface at each of the one or more other components, based on the completion of the bus activity.

12. The method of claim 10, further including

synchronizing the enabling signal to a system clock that is common to the bus structure.

13. The method of claim 10, further including

establishing a communications path between the component that initiated the bus activity and a target component of the one or more other components, and

enabling the bus interface at the target component within a time duration required to establish the communications path.

14. The method of claim 13, wherein

the enabling of the bus interface is independent of establishing the communications path.

15. An electronic circuit comprising:

a plurality of initiators that are configured to selectively initiate data-transfer operations via a bus structure,

a plurality of targets that are configured to process the data-transfer operations,

each of the plurality of targets including an interface for receiving the data-transfer operations, and

an activity detector that is configured to detect an initiation of a data-transfer operation from any of the plurality of initiators, and to generate therefrom an enabling signal, wherein

the interface of each of the plurality of targets is configured to receive the data-transfer operations in dependence upon the enabling signal from the activity detector.

16. The electronic circuit of claim 15, wherein

the plurality of initiators are configured to effect the data-transfer operations at a system clock speed, and

the interface of each of the plurality of targets is configured to operate at the system clock speed only when the activity detector provides the enabling signal.

17. The electronic circuit of claim 16, wherein

the enabling signal includes a clocking signal that operates at the system clock speed.

18. The electronic circuit of claim 15, wherein

the activity detector is further configured to detect the completion of the data-transfer operations, and to terminate the generation of the enabling signal based on the completion of the data-transfer operations.

19. The electronic circuit of claim 15, further including

a bus controller that is configured to establish a communications path between an initiator of the plurality of initiators and a target of the plurality of targets, wherein

the activity detector is configured to generate the enabling signal within a time duration required by the bus controller to establish the communications path.